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Implementation and Optimization of planar magnetics in the active balancer BMS DC/DC converter circuit. Current Probing challenges and techniques.

Analog designers often have need to accurately measure electric current in their circuits. There are some situations when simple voltage measurements will not give you desired information, and just inserting small value resistor to create artificial test point to monitor current is either impractical or impossible. While current measurements are relatively straight forward in loose and accommodating lab prototype, it becomes more challenging on finished printed circuit board, especially with currents flowing through traces routed in inner layers.

Good example of such circumstances is my recent work on the active balance BMS front end's key component - bidirectional synchronous flyback DC/DC converter, which is subject of this application note. The design task was to optimize characteristics of deployed planar transformer which replaced its traditional wire wound counterpart. Advantages and shortcomings of planar magnetics vs. wire wound ones are well understood and published, and are not subject of this note. Other than transformer optimization details for this particular application, we will focus on some encountered current measurement challenges and techniques that applicable not only to DC/DC converters or inductive components in particular, but to any analog circuit in general - line drivers, amplifiers, power supplies and such.

There are several methods to observe and measure electric current in a conductor, preferably without inserting resistive element that converts current to voltage. The most common tools are Hall effect sensor current probes, Rogowski coils (if the DC component is not relevant), and less known Positional current probes based on special design of a fluxgate magnetometer discussed further down. All these tools have to rely on indirect current measurement - they measure magnetic field strength which is proportional to the current flowing through the conductor, and, if calibrated properly, allow you not only observe the shape of a current waveform, but also make meaningful measurements of its value.

In my case I needed to observe on the scope and measure timing of current ramps through the primary and secondary windings of standard wire wound transformer used in a BMS Active Balancer reference application circuit, and compare these measurements to the flavor of the same circuit deploying planar transformers instead. This particular design is based on Linear Technology's very good LTC3300 active balancer controller IC - the first of this kind developed by LTC for use in high efficiency Battery Management Systems meant for managing lithium battery. The IC contains six controllers to implement

synchronous bi-directional flyback DC/DC converters capable of transferring energy from (to) a single cell to (from) the string of 6...12 cells connected in series. It also contains specialized interface circuitry. A fragment (one channel) of the DC/DC converter circuit suggested by LTC and subject of this work is presented on fig. 1. Complete design files are freely downloadable from Linear Technology's website.
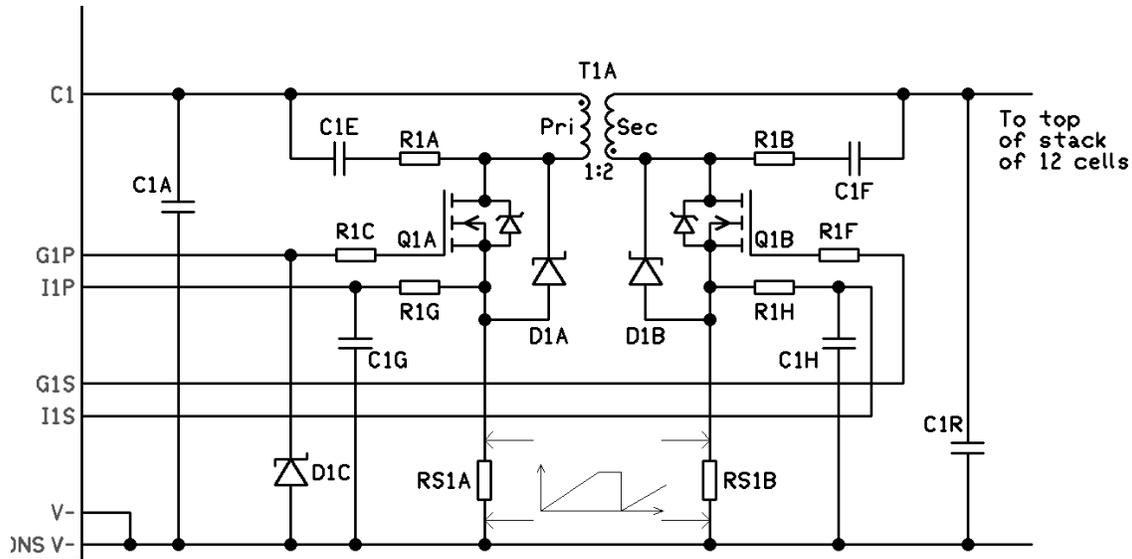

Fig.1. Suggested bi-directional synchronous flyback converter circuit schematic.
On the left a fragment of the LTC3300 BMS active balancer IC is shown.

Amount of external components in each of six converters is minimal for bi-directional capability - just two switching FETs, two sense resistors and shared transformer with two RC snubber networks. To set the maximum peak current flowing through transformer T1A windings, this design uses fixed sense resistors RS1A and RS1B in sources of respective FETs Q1A and Q1B. When the LTC3300 gets command to initiate charge transfer, it turns FETs on in sequence depending on the direction of charge transfer, one at the time. The current in respective transformer winding (and so the voltage drop on sense resistor) starts ramping up, and when the sensed voltage drop on RS1A or RS1B reach fixed 50mV threshold as sensed on IC's inputs I1P and I1S, the respective driver turns FETs off. User can set desired peak current (and so balancer's transfer power) by adjusting values of these sense resistors, while transformer's windings inductances primarily determine the slope of the current ramp and thus operating frequency. With adequately rated FETs and transformer this circuit can handle up to 10 A of current in or out of any single cell going out of (or into) the string of series cells. The charge transfer can be activated independently and simultaneously to/from one or few (or all) cells, which makes the circuit quite flexible in implementing sophisticated balancing algorithms. The IC is not a processor, it has no memory (other than memory for current command) and is basically nothing more than a

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collection of six remote controllable DC/DC converters driving external power stages + special SPI interface periphery.

To make sure converters operate properly and reliably, current ramps in transformer windings have to be checked out for linearity, magnitude and absence of parasitic oscillations. How to monitor these current ramps? A few tools mentioned above can do the job, but as always, the devil is in details.

Nothing beats accuracy and bandwidth of a quality Hall effect current probe, such as Tektronix A6302 shown on fig. 2, or similar.
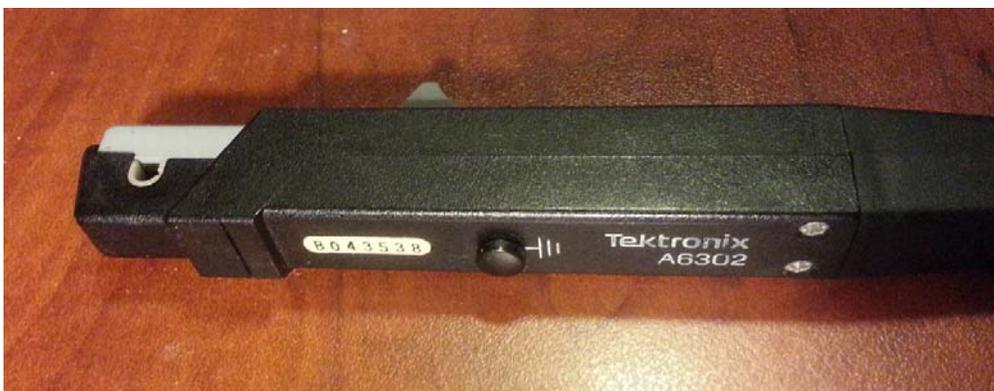

Fig.2 Tektronix A6302 current probe (the accompanying Tek AM503B amplifier is not shown).

A couple of such probes hooked to two channels of a four channel scope and observation of FET's drain voltages using two other channels will give you full picture of converter's health. Evaluating current ramps in primary and secondary windings of the flyback transformer is critically important step in validating your converter design. There is really no other way to confirm you're staying in linear flux density region (away from, magnetic core saturation) at maximum load. Knowing this is
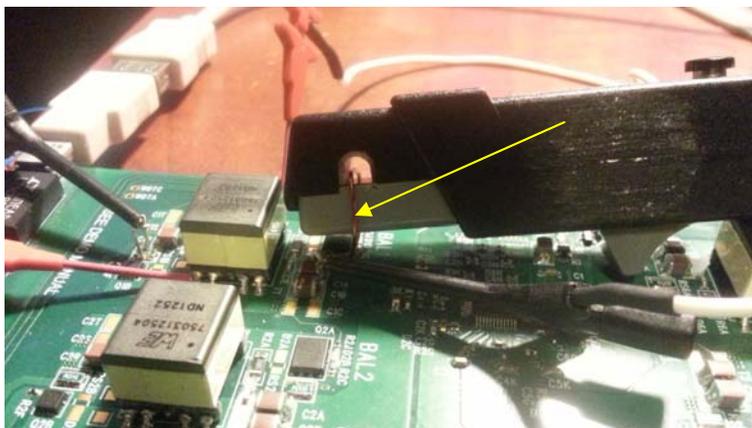

Fig. 3. Probing with A6302 requires cut PCB traces and inserting a wire loop – impossible task if traces are routed on inner layers.

Fig.4. Wire wound transformer design (fragment of Linear Technology Corporation's 2100A active balancer demo circuit)

Fig.5. Planar transformer based design (fragment of Metric Mind corporation's M17 active balancer prototype PCB)

necessary to avoid loss of efficiency, core overheating and "mysterious" blow ups of switching transistors due to huge peak currents resulting from lost inductance of saturated core. This may happen in marginal design if the load current or core rise temperature is miscalculated.

In early initial loose lab prototype it may be simple enough to find suitable place to insert a wire loop to clamp the probe around for such measurement (fig. 3), but it might be difficult or often impossible to accommodate on finished multilayer PCB especially if trace to be cut is on inner layer[1]. That, however, might be the least of the trouble. If you insert temporary wire loop for current measurement purpose while constructing a DC/DC converter running at >100kHz switching frequency, at best extra inductive loop will alter operation of the converter, and at worst it just may stop functioning all together. Remember that the locked current probe not only introduces Ohmic insertion loss in the wire but also greatly increases insertion inductance of the parasitic one-turn coil since probe's high permeability magnetic material now acts as its core. In marginal designs (or specific ICs) the converter may still work with bare wire inserted in the PCB for measurements, but normal operation will collapse as soon as probe head is locked around the wire. You must strive to minimize parasitic inductance of the ground path ! Transformer design is critical, and it is just not possible to mock up the circuit on the bench, get converter to work, and expect the same once design is transferred to a PCB. This sometimes limits usability of such current probes, especially with dense multilayer layouts such as shown on fig. 4 and fig. 5 - there is just no conductor loop in

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[1] Granted, we're discussing cases where inserting simple resistive shunt for current monitoring is not an option. Disrupting ground path by even small value resistor often prevents proper converter operation.

place to clamp such a probe around. It might seem that having sense resistors makes observing and measuring these currents simple by just monitoring voltage drop on them, however even if circuit will still function, connecting a scope to these resistors requires close attention to details, and success depends on your understanding of the current paths, shielding, grounding loops, parasitic influence of probe leads etc.

Consider this: In LTC's demo circuit primary winding sense resistor has value of just 8 mOhm, so the peak switching current is set to 0.05 V / 0.008 Ohm = 6.25 A by design. Without careful layout this kind of current will easily induce 50mV parasitic voltages on every few cm of non-terminated near-by conductor including scope test leads. I have made adapters with micro grip clips at the ends that are well

Fig. 6. This type of scope leads extension is absolutely unsuitable for high sensitivity probing.

suitable for troubleshooting digital logic circuits - they easily grab leads of a SOIC package with 1.27mm lead pitch (Fig.6). But if you try to grip by such adapter the ends of the low value sense resistor in a hope to see nice voltage ramp on it representing 6.25A peak currents flowing through the PCB traces, - forget it. Large current swings make each cm of PCB track act as miniature antenna transmitting this signal everywhere in near space, not to mention capacitive coupling to other near-by traces on the PCB. A 15cm of signal wire and 15cm of ground return wire on the scope probes form (meant for testing large PCBs)

form perfect antenna receiving parasitic signal resulting in far more than 50mV noise and ringing on the input, even if the signal and ground grips are shorted together. Fig. 7 shows what you will see.

Obvious solution, other than shorter traces reducing radiated interference, is to make probing tips and grounding leads as short as possible, but this still has its limitations. Unless you have active probe with integrated amplifier so the scope input can be 50 Ohm terminated, the next best way to handle this situation is to make ground and signal contact to the PCB right from the ring and tip of the probe without any wire extensions. Drastic improvement probing the same signal at very same test points without long leads is shown on

Fig. 7. Testing sense voltage with too long leads extension is practically useless.

Fig.8. It looks even better than LT's own waveform capture shown on fig. 15 (left side).

Fig. 8. Testing sense voltage (cyan trace) with direct connection of test leads to the current sense resistor.

Still, there was a lot of parasitic ringing caused by LC tanks formed by probe lead inductance and the scope input capacitance. Ideal solution for this would be coaxial test point connection where you connect the center conductor and the shield of the coax cable directly across sense resistor. This would preserve highest signal fidelity but would be totally impractical for a converter without sense resistors.

We're not going to discuss using Rogowski coils here because we're interested in measurements down to DC level. Besides, similar to the Hall effect current probe, such coil requires to be wrapped around current carrying conductor.

Miniaturized Rogowski coils have been made small enough to fit between leads of a TO220 case (fig.9.) and one can get creative and wrap it around the transformer lead, but the issue of having to cut PCB traces still remains. SMT transformers have no leads you can wrap Rogowski coil around of. But, like Hall effect sensors, they are pointless if you have option to monitor ramp currents by monitoring voltage drop on sense resistors. Other serious limitation of small Rogowski coils is limited low frequency response - because it works on HF transformer principle and picks up signal proportional to the rate of change of magnetic field crossing it, when AC current frequency approach DC, the rate of change drops so that declining coil response makes this method unusable below few hundred Hertz. Just like conventional transformer, it will not respond to DC current at all.

9. Miniature Rogowski coil

Fig. 10. Positional current probe

The very best practical measuring solution for observing and measuring currents in PCB tracks without disturbing them and dealing with large insertion losses is positional current probe (fig.10). As mentioned above, this type of probe

consists of a fluxgate magnetometer and signal conditioning circuit. It allows to pick up static magnetic fields, meaning the lowest response frequency is DC, just like for the Hall effect probes. As far as I'm aware, this is very first time a magnetometer core was miniaturized to the point that it fits into the insulated tip of the instrument that is just 2.6 mm wide. It is specifically meant to probe current in PCB traces, thus this unique instrument deserves a bit more elaborated description.

Same as for Hall effect sensor type, its operation relies on the fact that every conductor (PCB trace included) carrying electric current creates magnetic field around it, which can be picked up, displayed and measured. The fundamental distinction from a Hall effect sensor though is that the fluxgate magnetometer's core does not have to enclose the conductor and form continuous magnetic path around it, and thus can measure the field strength in any point in space, including one side of a wire or, say, a PCB trace. Because the sensor measures absolute external magnetic field strength, not density of flux lines, it does not require closed magnetic path as a Hall effect sensor does.
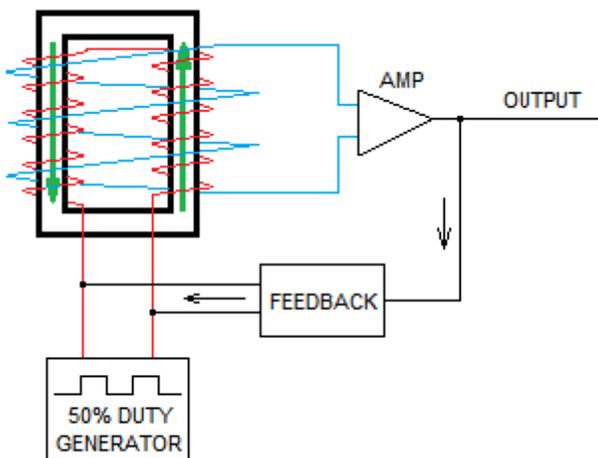
To elaborate on the working principle of the fluxgate magnetometer (fig.11), is quite simple: a 50% duty cycle rectangular pulse generator feeds the coil (shown in red) driving magnetometer's tiny core into deep saturation at high frequency (40...50 MHz), causing it to follow classic B-H curve (flux density B as function of magnetizing force H). On each cycle direction of magnetic flux (green arrows) reverses to the opposite. A sense coil (blue) wound and centered around whole core is connected to the amplifier whose output is fed back to the driving coil (some designs use third "compensating" coil for that purpose). In the absence of external magnetic field the B-H curve is completely symmetric. Total excitation currents driving the sensor core in saturation in both directions is also symmetrical, so the core spends equal time in positive and negative quadrants of its saturation graph. The magnetic field created by each green flux line is the same so the currents induced in common sensing coil by the fields oriented in opposite directions cancel out, and the sensor output reads zero. However, any external magnetic field near current carrying conductor biases (pre-magnetizes) the core, so it will reach saturation sooner and thus spends more time in one quadrant of its saturation graph than in the other resulting in non-zero net current induced in the sense coil. An amplifier drives the feedback circuit that feed driving (or field compensating coil) creating magnetic field exactly opposite to the external disturbing field thus restoring symmetry, until the sense coil reads zero again. In other words compensating field cancels out external field we're interested in. Amount of the compensation current (which is output of the instrument) required to do that is exactly

proportional to this external field strength, so it can be quantified after calibrating the sensor.
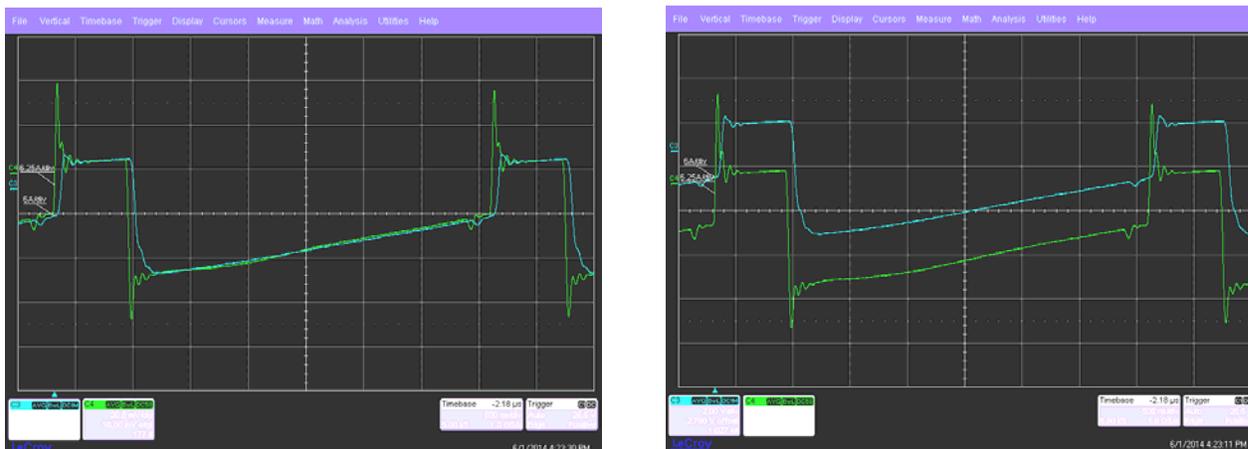

Fig.11. Signal waveforms obtained from the same conductor by A6302 and 520 current probes.

The bandwidth of this probe is effectively ~10x lower than the excitation frequency, and for this particular model 520 probe is somewhat limited - 5 MHz. This means any high order harmonics of a DC/DC converter running at ~100 kHz switching frequency will be attenuated and eventually "lost". Also, due to limited frequency response the output signal will be few tens of nanoseconds delayed. Think of it as a low-pass filter with 5 MHz cutoff

frequency. However, all relevant details of the sensed signal up to this frequency will be preserved and ability to see and measure current running trough any conductor or a PCB track just by touching it more than compensated for these shortcomings. Limited bandwidth may, in fact, be quite advantageous to filter out unwanted parasitic noise. Fig. 11 illustrates the difference between 5MHz bandwidth I-prober 520 (cyan trace) and 50 MHz Tektronix A6302 Hall effect probe (green trace) as they reproduce shape of current passing through the very same conductor. The A6302 is clamped around the wire and 520 is just touching it (fig.12). On the right snapshot the same

Fig.12. This setup simultaneously captured is waveforms shown on fig. 11.

signals are shown with vertical offset deliberately introduced for clarity. Nearly 100 ns signal delay and some fidelity loss for the 520 magnetometer type positional probe vs. 10 times faster [and thus 4 times more expensive...] A6302 Hall effect probe is clearly visible.

Using positional current probe to see and measure current flowing through a PCB track is just as simple as seeing and measuring voltage - just touch the track with its insulated probe tip[1].

Because the current measurement is contactless, in fact it is more versatile since you can see and accurately test current flowing through the trace routed on inner layers - something you cannot do for voltage measurements requiring direct electrical contact.

The 520 probe allowed me to obtain current ramp information straight from SMT current sensing resistors by simply touching their top surface (fig.13).

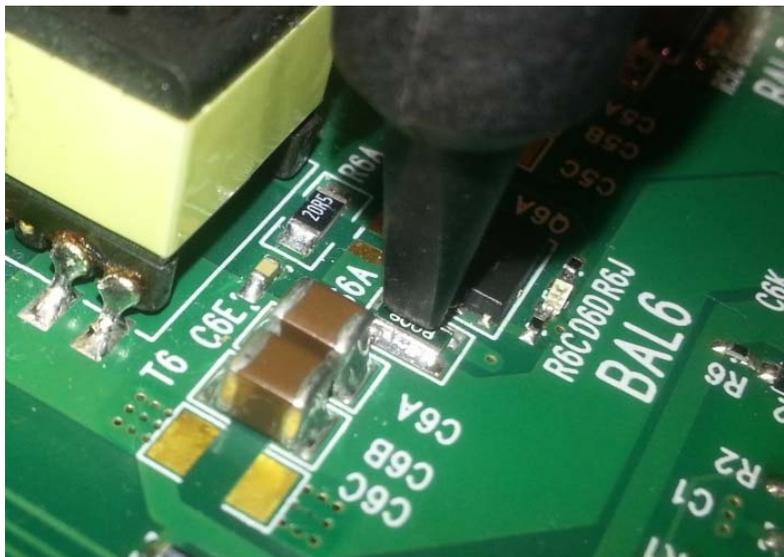Fig.13. Using positional current probe

Fig. 14. picking up current through the sense resistor

There was no single conductor trace narrow enough carrying entire winding current because the large copper pour for this conductor was deployed to increase ground side of sense resistor area, and also because direct wide copper strip from the sense side of the SMT resistor to the source of switching FET was wider than the tip of the probe. But since all sense current is concentrated to flow through the resistor itself, the field density around it is maximum and signal quality picked up from its surface was the best. Fig. 14 depicts zoomed in view of probing the current through the RS1B SMT sense resistor (see schematic on fig. 1).

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[1] Provided, the probe is calibrated prior to taking measurement. Calibration is tricky.

Final test done on the 2100A Active Balancer Demo Circuit was to compare actual data as published by Linear Technology Corporation in the Demo Manual for this circuit and the data I actually captured from very the same board using the 520 positional current probe. The comparison is presented on fig. 15. Note lack of ringing for the plot lines depicting current ramps.

Now that the current measurement problem is sorted out, let's come back to the planar magnetics and transformer optimization issue. Initially calculated transformer parameters were used to create layout and build the prototype circuit M17 (Metric Mind's 17th BMS design - sequential numbers are assigned to each new hardware iteration). Fragment of the M17 PCB is shown on fig. 5. The circuit worked well right "out of the box".

LTC test data. Top - charge cell, bottom - discharge cell.   MMC test data. Top - charge cell, bottom - discharge cell.
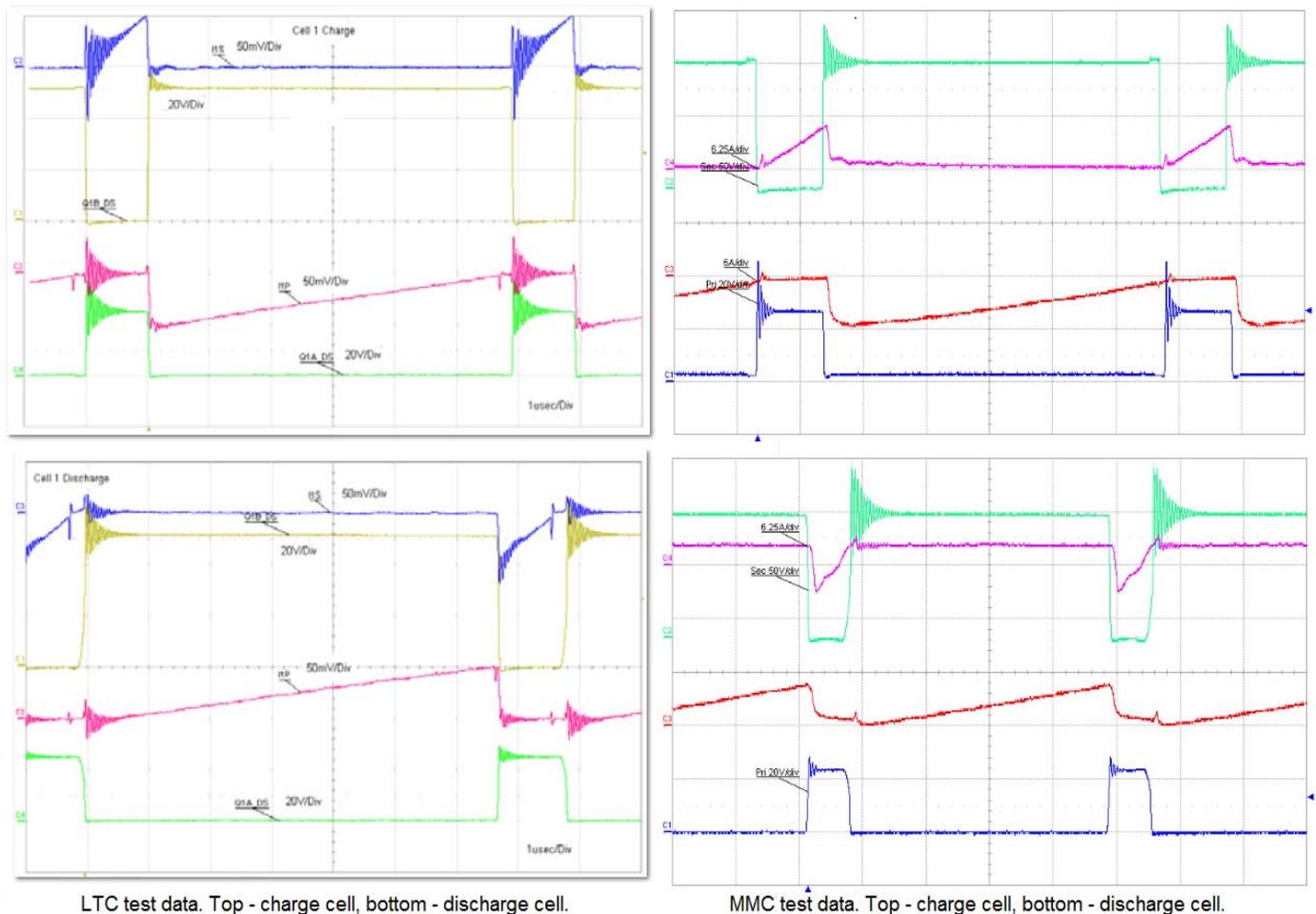
Fig. 15. Comparison of the test data collected by LTC and MMC on the same hardware. MMC waveforms were captured on LeCroy WaveSurfer 424 four channel 200MHz oscilloscope.

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After confirming that no transformer saturation takes place, several iterations of the windings configurations were attempted, each time recording switching FET's drain voltage waveform and operating frequency. Initial switching frequency with planar transformers shown on fig. 5 was 118 kHz during charging and 117 kHz during discharging (12 cells in series on the secondary side).

The idea was to try to reduce amount of turns in windings and see how turns ratio affects converter operation. Few combinations of the winding turns worked well - the converter was chocking only at the extremes (just 1 turn for the primary and >6 turns for secondary winding). Minimizing amount of turns reduces mutual capacitance, but there is a risk to have unacceptably high operation frequency (beyond the LTC3300 capability) due to increased ramp slope while still having the same fixed peak current guaranteeing no core saturation. With only 3 primary and 6 secondary turns there is not that much flexibility to maintain desired 1:2 turns ratio - there are only so many integer ratios available between 1:1 and 1:2 practical limits for this design. If two turns are too few and three are too many for desired inductance, the only way to adjust inductance it is to vary the core gap. The E22 size 3F3 or 3C90 core material comes with a few standard pre-made gaps, with two largest ones designated as A630 and A400 parts.

The next task was to alter transformer design to get it closer to the Würth 750312504 wire wound reference counterpart used by LTC on their demo circuit. The reason for this is that the demo circuit was able to pump in and out around 2.4 A while M17 circuit had average cell current variations among its 12 converters between about 1 A and 2.5 A. Considering very consistent transformer geometries, this suggested that either converter operation is marginal in some respect, or the tolerance of some components (most likely sense resistors) has too wide variation. Now that the measurement technique is refined, it will be easy to go around all 12 converters and check them out for consistency.

As I mentioned, in this particular balancer circuit design LTC used off-shelf Würth 750312504 transformers which have 3.16uH primary and 12.6uH secondary winding inductance respectively. After a few iterations optimal core gap and windings configuration were found to mimic this transformer very closely using E22 size E-I planar magnetic core (this size was picked up based on max power it can handle), The only difference was about 4x inter-winding capacitance for the planar transformer (153 pF) vs. wire would Würth 750312504 counterpart (39pF). The very clean oscillogram shown on fig.6 was obtained from the DC/DC converter on M17 PCB using this very flat planar core for its transformers.

Excessive inter-winding capacitance will cause current spike at the beginning of the current ramp after FET switches on. This can be seen on fig. 16 (green trace, the scale is actually 3.125A/div). Naturally, this spike was found to be more pronounced in the DC/DC converter implemented with planar transformer. The only concern here is not to allow corresponding voltage spike on the sense resistor to exceed 50mV after first 60ns of the ramp (LTC3300's built-in sense line blanking time), as such a spike will shut down

switching FET prematurely, thus reducing average balancing current and making it unstable. Because of inconsistent average current for some of 12 DC/DC converters in this initial design, the next step is to check all 12 converters for the presence and magnitude of the transformer current spike (and so the corresponding voltage spike on sense resistors) as it could be responsible for reduced average transfer current. Based on the plot on fig. 15 and fig. 16 the spike is quite far below 50mV level, so planar magnetics do not present any issues for proper LTC3300 operation. There is always an option to adjust or improve simple filtering implemented with R1G-C1G and R1H-C1H components (see fig. 1 schematic) if voltage spikes need to be suppressed further. One should note that with only 0.008 Ohm sense resistor consistency of solder joints, copper thickness and power trace geometry can easily alter total resistance and so the voltage seen by LTC3300's sense amps, not to mention tolerance of resistors themselves. This may partially be responsible for inconsistent power transferred by different DC/DC converters on M17 prototype PCB. Such inconsistency was also noticed on the LT's 2100A Demo circuit board, albeit to lesser degree.
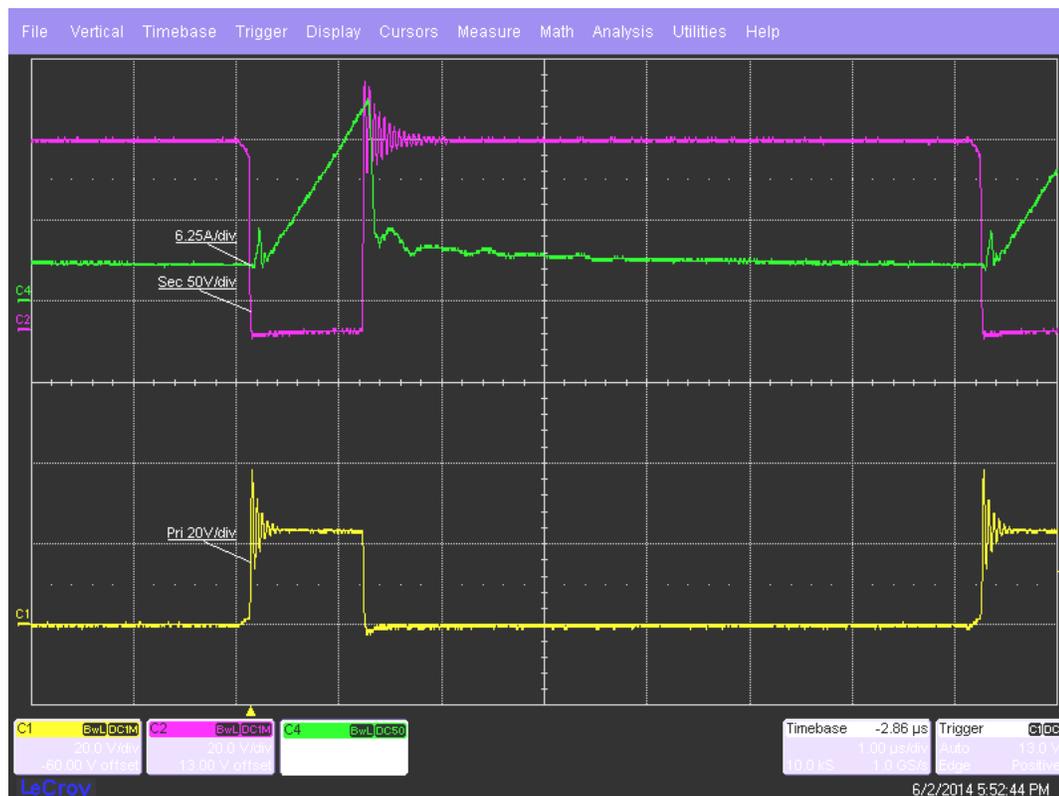

Fig. 16. M17 prototype with planar transformer. linear current ramp (green trace) up to sense amp threshold level. About 500 mA initial current spike caused by inter-winding capacitance is visible. No core saturation observed.
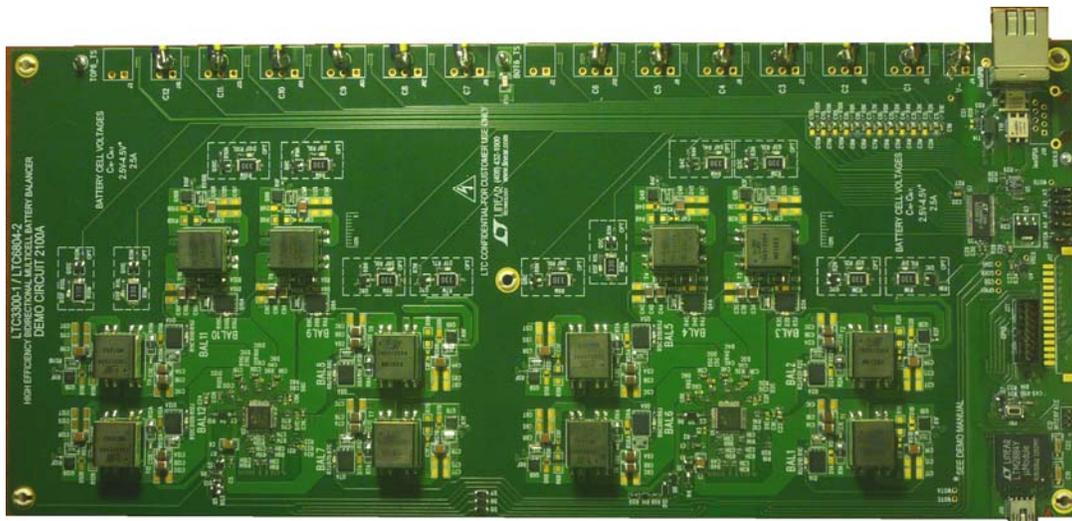
DENT #003 will discuss the test software, and final achieved performance of the active balancer based on the LTC3300 controller chip and planar magnetics. This includes evaluation and tests of the LTC6804-2 voltage monitor and board-to-board communication. Signal isolation is achieved using smaller planar transformers handling LT's pulse modulation method. Stay tuned.
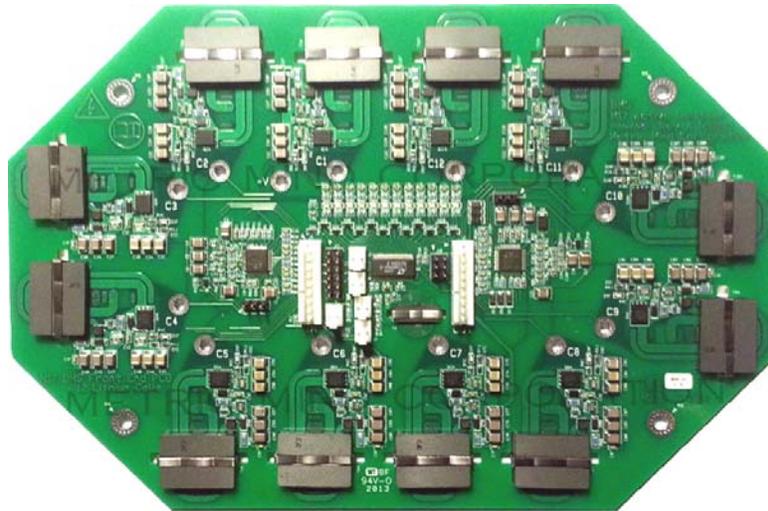
MMC M17 Active Balancer prototype PCB

LTC 2100A Active Balancer Demo Circuit - both photos are the same scale.

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